Attorney Docket No.: CYPR-CD00232

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Warren Snyder

Application No.: 10/033,027 Group Art Unit:

Filed: 10/22/01 Examiner:

Title: PROGRAMMABLE MICROCONTROLLER ARCHITECTURE

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,460,172	10/01/02	Insenser Farre et al.	716	17	06/21/00

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	B							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00232

Inventor(s): Snyder

Group Art Unit: 2183

Filed: October 22, 2001

Examiner: PAN, Daniel H.

Application No.: 10/033,027

Confirmation No.: 8635

Title: PROGRAMMABLE SYSTEM ON A CHIP

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,399,922	MACROCELL COMPRISED OF TWO LOOK-UP TABLES AND TWO FLIP-FLOPS	Mar. 21, 1995
5,680,070	PROGRAMMABLE ANALOG ARRAY AN METHOD FOR CONFIGURING THE SAME	Oct. 21, 1997

FOREIGN DOCUMENTS

Document No.:	Title:	Publ. Date
EP 0 450 863 A2	INTEGRATED CIRCUIT FOR ANALOG SYSTEM	Oct. 9, 1991
EP 0 499 383 A2	MIXED MODE ANALOG/DIGITAL PROGRAMMABLE INTERCONNECT ARCHITECTURE	Aug. 19, 1992
EP 0 308 583 A2	DIGITAL COMPUTER HAVING SIGNAL CIRCUITRY	Mar. 29, 1989
EP 0 639 816 A2	FIELD PROGRAMMABLE DIGITAL SIGNAL PROCESSING ARRAY INTEGRATED CIRCUIT	Feb. 22, 1995

04/11/05

EP 1 170 671 A1	PROGRAMMABLE ANALOG ARRAY CIRCUIT	Jan. 9, 2002
PCT WO 95/32478	INTEGRATED CIRCUIT HAVING PROGRAMMABLE ANALOG FUNCTIONS AND COMPUTER AIDED TECHNIQUES FOR PROGRAMMING THE CIRCUIT	Nov. 30, 1995

OTHER DOCUMENTS

Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.

Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.

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Respectfully submitted,

04/11/05

Date: April 6, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00232

Inventor(s):	Warren Snyder		
Serial No.:	10/033,027	Group Art Unit:	
Filed:	10/01/01	Examiner:	
Title:	PROGRAMMABLE SYSTEM ON A CHIP		

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

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The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,144,327	PROGRAMMABLY INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93
5,880,598	TILE-BASED MODULAR ROUTING RESOURCES FOR HIGH DENSITY PROGRAMMABLE LOGIC DEVICE	03/09/99
6,304,101	PROGRAMMABLE LOGIC DEVICE, INFORMATION PROCESSING SYSTEM, METHOD OF RECONFIGURING PROGRAMMABLE LOGIC DEVICE AND METHOD COMPRESSING CIRCUIT INFORMATION FOR PROGRAMMABLE LOGIC DEVICE	10/16/01
5,426,378	PROGRAMMABLE LOGIC DEVICE WHICH STORES MORE THAN ONE CONFIGURATION AND MEANS FOR SWITCHING CONFIGURATIONS	06/20/95
5,828,693	SPREAD SPECTRUM FREQUENCY HOPPING READER SYSTEM	10/27/98
5,703,871	FACILITATES DATA LINK HANDLER IN A PERFORMANCE MONITORING AND TEST SYSTEM	12/30/97
6,018,559	CHAIN-CONNECTED SHIFT REGISTER AND PROGRAMMABLE LOGIC CIRCUIT WHOSE LOGIC FUNCTION IS CHANGEABLE IN REAL TIME	01/25/00
6,191,660	PROGRAMMABLE OSCILLATOR SCHEME	02/20/01
5,939,949	SELF-ADJUSTING STARTUP CONTROL FOR CHARGE PUMP CURRENT SOURCE IN PHASE LOCED LOOP	08/17/99
6,157,270	PROGRAMMABLE HIGHLY TEMPERATURE AND SUPPLY INDEPENDENT OSCILLATOR	12/05/00
4,138,671	SELECTABLE TRIMMING CIRCUIT FOR USE WITH A DIGITAL TO ANALOG CONVERTER	02/06/79
5,633,766	MAGNETIC DISK STORAGE APPARATUS WITH PHASE SYNC CIRCUIT HAVING CONTROLLABLE RESPONSE CHARACTERISTICS	05/27/97
6,166,367	PROGRAMMABLE ANALOG ARITHMETIC CIRCUIT FOR IMAGING SENSOR	12/26/00
5,600,262	INTEGRATED CIRCUIT FACILITATING SIMULTANEOUS PROGRAMMING OF MULTIPLE ANTIFUSES	02/04/97

04/16/03

02/21/03

5,414,308	HIGH FREQUENCY CLOCK GENERATOR WITH MULTIPLEXER	05/09/95
5,258,760	DIGITALLY DUAL-PROGRAMMABLE NTEGRATOR CIRCUIT	11/02/93
5,563,526	PROGRAMMABLE MIXED-MODE INTEGRATED CIRCUIT ARCHITECTURE	10/08/96
6,225,866	SERIES CONNECTED MULTISTAGE LINEAR FET AMPLIFIER CIRCUIT	05/01/01

The Examiner's attention is respectfully directed to the following Related Pending U.S. Patent Applications:

CYPR-CD00169; "PROGRAMMABLE MICROCONTOLLER ARCHITECTURE (MIXEDANALOG/DIGITAL)"; 08/07/01; 09/924,734; Snyder et al.

CYPR-CD00170; "DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,045; W. Snyder

CYPR-CD00172; "CONFIGURING DIGITAL FUNCTIONS IN A DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,109; W. Snyder

CYPR-CD00173; " A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; M. Mar

CYPR-CD00174; "PROGRAMMING METHODOLOGY AND ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM (AS AMENDED)"; 08/14/01; 09/930,021; Mar et al.

CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam

CYPR-CD00180; "METHOD AND APPARATUS FOR PROGRAMMING A FLASH MEMORY"; 06/05/01; 09/875;599; W. Snyder

CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE"; 10/10/01; 09/975,115; Snyder et al.

CYPR-CD00187; "A CONFIGURABLE INPUT/OUTPUT INTERFACE FOR A MICROCONTROLLER"; 09/14/01; 09/953,423; Kutz et al.

CYPR-CD00199; "MULTIPLE USE OF MICROCONTROLLER PAD"; 06/26/01; 09/893,050; Kutz et al.

CYPR-CD00226; "PROGRAMMING ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM"; 08/14/01; 09/929,891; Mar et al.

CYPR-CD00227; "ARCHITECTURE FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE ANALOG PROGRAMMABLE ANALOG BLOCKS"; 10/01/01; 09/969,313; B. Sullam

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04/14/08